What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the N-type MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

2. The semiconductor device as defined in claim 1,

wherein the impurity concentration of the third diffusion region is set to a value enabling a breakdown start voltage of the Zener diode to be lower than a breakdown start voltage of the MOS transistor.

3. The semiconductor device as defined in claim 1, wherein:

an NPN lateral bipolar transistor is formed by the first and second diffusion regions which are N-type diffusion regions and a P-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is an N-type MOS transistor which sets a potential of a pad to a low potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is a P-type diffusion region.

4. The semiconductor device as defined in claim 1, wherein:

a PNP lateral bipolar transistor is formed by the first and second diffusion regions which are P-type diffusion regions and an N-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is a P-type MOS transistor which sets a potential of a pad to a high potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is an N-type diffusion region.

5. The semiconductor device as defined in claim 1, further comprising:

a fourth diffusion region which is provided between the silicide layer and the third diffusion region and makes up a Schottky diode together with the silicide layer.

6. The semiconductor device as defined in claim 3, further comprising:

fourth and fifth diffusion regions formed between the silicide layer and the third diffusion region,

wherein the third, fourth, and fifth diffusion regions make up a PNP bipolar transistor.

7. The semiconductor device as defined in claim 4, further comprising:

fourth and fifth diffusion regions formed between the silicide layer and the third diffusion region,

wherein the third, fourth and fifth diffusion regions make up an NPN bipolar transistor.

8. A method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the

semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type and N-type wells near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, in a region near the second isolation region and a deeper part of the first diffusion region; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions.

9. The method of fabricating a semiconductor device as defined in claim 8,

wherein the impurity concentration of the third diffusion region is set to a value enabling a breakdown start voltage of the Zener diode to be lower than a breakdown start voltage of the MOS transistor.

10. The method of fabricating a semiconductor device as defined in claim 8, further comprising:

a step of forming a fourth diffusion region which is provided between the silicide layer and the third diffusion

region and makes up a Schottky diode together with the silicide layer.

11. The method of fabricating a semiconductor device as defined in claim 10,

wherein the third and fourth diffusion regions are formed by forming a mask on the semiconductor substrate and using the mask to dope the semiconductor substrate with impurities.

12. The method of fabricating a semiconductor device as defined in claim 8, wherein:

an NPN lateral bipolar transistor is formed by the first and second diffusion regions which are N-type diffusion regions and the P-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is an N-type MOS transistor which sets a potential of a pad to a low potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is a P-type diffusion region.

13. The method of fabricating a semiconductor device as defined in claim 12, further comprising:

a step of forming fourth and fifth diffusion regions between the silicide layer and the third diffusion region,

wherein the third, fourth, and fifth diffusion regions

make up a PNP bipolar transistor.

14. The method of fabricating a semiconductor device as defined in claim 12, wherein:

a P-type MOS transistor which sets the potential of the pad to a high potential is further provided;

a diffusion resistance connected between a drain of the P-type MOS transistor and the pad is provided; and

the diffusion resistance is formed in the step of forming the third diffusion region.

15. The method of fabricating a semiconductor device as defined in claim 8,

a PNP lateral bipolar transistor is formed by the first and second diffusion regions which are P-type diffusion regions and the N-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is a P-type MOS transistor which sets a potential of a pad to a high potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is an N-type diffusion region.

16. The method of fabricating a semiconductor device as defined in claim 15, further comprising:

a step of forming fourth and fifth diffusion regions

between the silicide layer and the third diffusion region,

wherein the third, fourth, and fifth diffusion regions make up an NPN bipolar transistor.

17. The method of fabricating a semiconductor device as defined in claim 15, wherein:

an N-type MOS transistor which sets the potential of the pad to a low potential is further provided;

a diffusion resistance connected between a drain of the N-type MOS transistor and the pad is provided; and

the diffusion resistance is formed in the step of forming the third diffusion region.

18. The method of fabricating a semiconductor device as defined in claim 13,

wherein the third, fourth and fifth diffusion regions are formed by forming a mask on the semiconductor substrate and using the mask to dope the semiconductor substrate with impurities.

19. The method of fabricating a semiconductor device as defined in claim 16,

wherein the third, fourth and fifth diffusion regions are formed by forming a mask on the semiconductor substrate and using the mask to dope the semiconductor substrate with impurities.

20. A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate;

a third diffusion region which is formed between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor; and

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.

21. The semiconductor device as defined in claim 20,

wherein the impurity concentration of the third diffusion region is set to a value enabling a breakdown start voltage of the Zener diode to be lower than a breakdown start voltage of the MOS transistor.

22. The semiconductor device as defined in claim 21, wherein:

an NPN lateral bipolar transistor is formed by the first and second diffusion regions which are N-type diffusion regions and a P-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is an N-type MOS transistor which sets a potential of a pad to a low potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is a P-type diffusion region.

23. The semiconductor device as defined in claim 21, wherein:

a PNP lateral bipolar transistor is formed by the first and second diffusion regions which are P-type diffusion regions and an N-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region is a P-type MOS transistor which sets a potential of a pad to a high potential; and

the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is an N-type diffusion region.

24. A method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type wells and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.